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A DEEP LEVEL TRANSIENT STUDY OF IMPURITY CENTRES IN MICROCRYSTALLINE SILICON OBTAINED BY HOT-WIRE CHEMICAL VAPOUR DEPOSITION

V. Schlosser, A. Breymesser
Institut für Materialphysik der Universität Wien
A-1090 Wien, Strudlhofgasse 4, Austria, phone: (+43 1) 586 34 0927, e-mail: viktor.schlosser@univie.ac.at

D. Soler, M. Fonrodona, C. Voz, J. Bertomeu
Departament de Física Aplicada i Òptica, Universitat de Barcelona
E-08208 Barcelona, Av. Diagonal 647, Spain.

ABSTRACT: We have investigated diode structures of microcrystalline silicon, deposited by hot-wire chemical vapour deposition, by means of the complex differential AC conductivity. An equivalent circuit model taking into account the two contributions to the conductance arising from the crystalline and the noncrystalline phase in the silicon films was used to derive information about the defect distribution in the microcrystalline silicon devices. The influence of slightly changing preparation conditions on the electrical behaviour of the samples was mainly caused by variations in the density of surface states at the crystalline grains. A substrate temperature of 230 °C during deposition was leading to a smaller contribution of the noncrystalline phase to the conductivity than observed for samples deposited at 200 °C. Changing the filament temperature from 1600 °C to 1800 °C reduces the uncompensated electrically active surface state density.
Keywords: Micro Crystalline Si - 1: Defect Density - 2: Capacitance -3

1. INTRODUCTION

In the past years large efforts were made to develop high efficient solar cells based on thin, crystalline silicon grown on or transferred to cheap foreign substrates [1]. The wide variety of methods reported so far essentially follow two approaches. The first approach is aiming at the preparation of silicon layers with large sized crystal grains (>100 µm in diameter) in order to minimise effects of grain boundaries. The design of the final solar cell is similar to the well experienced *pn*-junction devices made from single crystal or multicrystalline silicon wafers. Modelling predicts short circuit current densities, open circuit voltages and therefore conversion efficiencies close to the values reported for high efficient solar cells prepared from single crystal silicon wafers. The second approach is the growth of nano- or microcrystalline silicon films (nc-Si, µc-Si) at substrate temperatures between room temperature and 400 °C with a similar technique currently used for the fabrication of amorphous silicon *pin*-solar cells. Due to the limited thickness of typically less than 5 µm and the weak absorption of light in the long wavelength region it is expected that the short circuit current density will always be somewhat reduced compared to high efficient solar cells even when an optimised light trapping structure is realised. The second potential drawback of microcrystalline devices is believed to be caused by the introduction of an undoped, intrinsic layer which does not allow to establish built in electric fields as high as known for abrupt *pn*-junctions. As a consequence the open circuit voltage should be lower than obtainable with *pn*-junction solar cells. Despite their potential restrictions solar cells made from nc-Si/µc-Si already have demonstrated efficiencies above 10% [1]. The major advantage of the preparation of µc-Si based solar cells is the simple, integrated deposition process of doped and undoped layers without the additional, critical high temperature treatment which is unavoidable when large grains have to be recrystallised or grown.

In the present work, we have investigated electrically active defects in diode structures of µc-Si grown by the hot-wire chemical vapour deposition process (HWCVD) using conductance and capacitance measurements in order to evaluate optimised preparation conditions of the absorbing layer thus leading to an adequate electrical quality of the intrinsic silicon layer in the final *pin*-solar cell.

2. EXPERIMENTAL

All diode structures have been prepared by HWCVD deposition using silane, SiH_4, diluted with hydrogen as source gas. Onto glass substrates coated with highly conducting zinc oxide, ZnO, which served as the back electrode in the final device, an about 50 nm thick, highly boron doped µc-Si layer was deposited by introducing *di*borane into the gas flow. Subsequently a 2 µm to 3 µm thick layer was grown without additional doping gases. On top of the nominally intrinsic µc-Si layer a matrix of chromium dots with 1 mm or 2 mm diameter and a spacing of 3 mm - 5 mm were evaporated, which served as ohmic front contacts. Transmission electron microscopy (TEM) images showed a needle-like growth of the crystals from the substrate surface. The diameter of the needles was in the range of 20 nm to 30 nm, with lengths exceeding 100 nm. The crystallites were embedded in a noncrystalline matrix [2]. We examined four samples which have been prepared with slightly different deposition conditions concerning the substrate temperature, the filament temperature and the filament material.

At room temperature, the frequency dependence of the complex differential AC conductance (capacitance and conductance) of the samples was recorded in the frequency range from DC up to 10 MHz. A lock in amplifier was used for frequencies up to 100 kHz and an impedance analyser above 1 MHz. During the frequency sweeps, the samples were kept at a fixed DC bias voltage which was in the range between –1 V and +1 V. The temperature dependent measurements of the AC conductance with an excitation amplitude of 30 mV_{rms} were carried out with a capacitance bridge at a fixed frequency of 1 MHz. Together with an external pulse generator the same capacitance bridge was used for deep level transient spectroscopy ex-

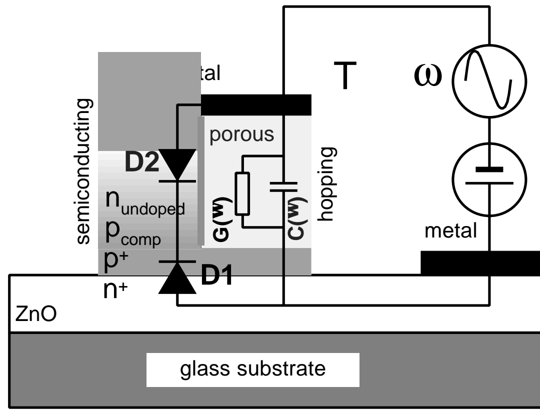

Figure 1: One dimensional model of the µc-Si structure. The noncrystalline fraction of the silicon film is described by a hopping conduction in parallel with the two space charge regions in the crystal. The first junction, D1, is given by the *n*-ZnO/*p*-Si transition, the second diode, D2, with opposite polarity occurs at the *p*-Si/undoped Si junction.

periments (DLTS). The temperature ranged from 80 K to 350 K. During the temperature sweep the samples were kept at a constant bias voltage. With respect to the two junctions which were present in our samples as shown in figure 1 an either positive or negative bias voltage was chosen and kept constant. That means that one of the two junctions was depleted whereas the other one was forward biased. For the data evaluation, the depleted junction was of interest. The capacitance and conductance were recorded as a function of the temperature. For the DLTS experiments, a short voltage pulse was applied and the capacitance transients were monitored. The pulse amplitude was varied. In most experiments the pulse duration was kept constant at 1 ms which was found to be long enough to completely fill the charge traps we have investigated. The capacitance transients which occured when carriers were released from the deep traps were used to evaluate the energy levels and the corresponding capture cross sections of electrically active defects located in the depletion region. The time resolution for the transient measurements was 10 µs. The rate windows used to obtain the DLT spectra were varied between several 10 µs up to 1 s. For each of the four samples at least three different chromium dots were chosen for the experiments.

3. RESULTS AND DISCUSSION

In order to interpret the data by the electrical properties of the crystallites and the noncrystalline fraction of the silicon films a model as shown in figure 1 was assumed. The electrical equivalent circuit in the noncrystalline phase was described by a capacitance and a conductance in parallel which is independent of the applied DC bias voltage. In the crystalline phase the circuit was modelled by two diodes assumed to be located at the *n*-ZnO/*p*-Si interface and at the transition from the highly doped *p*-Si to the undoped Si region. Due to the space charge regions at the two junctions these two diodes will represent two voltage dependent capacitors in series. The parts of the two circuits are connected in parallel by the front and the back contact. The frequency dependent measurements of the AC conductance showed that the real part (conductance) of the devices remains nearly constant at low frequencies up to several kHz, then the conductance starts to increase with frequency. A log-log plot of the conductance versus frequency suggests a power law for the conductance above 10 kHz with an exponent between +0.3 and +0.5. This dependence is characteristic for a hopping conduction mechanism which can be expected in highly disordered materials. At low frequencies, the conductance is governed by the diodes in the crystalline fraction of the layers and exhibits a clear dependence on the applied DC bias voltage. The dependece almost vanishes once the excitation frequency is raised above 1 Mhz which suggests that there is no rectifying junction in the noncrystalline phase. From the observed frequency dependence of the samples we conclude that the influence of the noncrystalline phase on the electrical DC properties is negligible and will not affect the solar cell characteristics of a *pin*-device.

The diameters of the crystallites are in the order of the characteristic Debye-Hückl length, L_D, of crystalline silicon region even for high doping concentrations (~10^{18} cm^{-3}). L_D determines the extension of a space charge region in the crystal caused by surface charges at the grain boundaries and therefore cannot be neglected for our samples. It is well known that surface states at grain boundaries introduce a high density of deep lying energy levels in the band gap [3]. In the case of fine grains the presence of surface states will result in an energy band bending which can exceed the length of half of the diameter of the grain. In this case the Fermi level is no longer determined by the doping concentration in the bulk crystal and a pinning of the Fermi level on the energy level of the dominant surface states takes place which is independent from the background concentration in the grains in a wide range. In a comparably shallow region of the background concentration a noticeable compensation effect can occur when the bulk contains charges with opposite sign compared with the surface charges, thus causing the Fermi level to rise from the pinned value towards the valence band or conduction band edge, respectively. For a uniformly distributed donorlike deep defect level in the bulk crystal the following equation describes the condition for complete compensation by introducing additional acceptors.

$$N_T^+ = n + N_A = \frac{N_T}{1 + \boldsymbol{b}^{-1} \exp\left[-\left(\boldsymbol{x} - E_T\right)/k_B T\right]} \qquad (1)$$

N_T is the donor concentration, n the concentration of free electrons, N_A the acceptor concentration, E_T the energy level of the donor, $\boldsymbol{b}$ the spin degeneracy factor and $\boldsymbol{x}$ given by

$$n = N_C F_{1/2}\left(-\boldsymbol{x}/k_B T\right) \qquad (2)$$

N_C is the effective density of states in the conduction band and $F_{1/2}$ is the Fermi-Dirac Integral. For the case $n << N_A$ the Fermi level, $\boldsymbol{e}_F$, is then given by

$$\boldsymbol{e}_F = \boldsymbol{e}_C - E_T + k_B T \ln\left[\frac{\boldsymbol{b}\left(N_T - N_A\right)}{N_A}\right] \qquad (3)$$

$\boldsymbol{e}_C$ is the energy of the conduction band edge. From Eq. 3 it can be seen that the Fermi level position does not depend on the energy level of the acceptor. As a consequence, all potentially present acceptors contribute equally to the compensation. A detailed analyses can be found in Ref. 4. In the case of surfaces, fixed charges are locally separated. The defects are located at the grain boundary

whereas the dopant is incorporated in the crystal matrix. Therefore, on a microscopic scale the Fermi level position is a function of the distance from the crystal surface.

In Fig. 2 the influence of the doping concentration on the band diagram for a small one dimensional crystal is illustrated. All units were arbitrarily chosen. The numerical calculation assumed a constant thickness of the crystal, d, with boundaries at x=0 and x=300, a constant donorlike defect density located at the boundaries with an energy level in the middle of the bandgap of silicon (0.56 eV). Mobile charges were neglected. The energy diagrams for three acceptor concentrations, uniformly distributed in the crystal lattice, are shown. In the case of a high doping concentration the space charge region at the grain boundaries only extends in a narrow region into the crystal causing a steep band bending at the boundaries then the valence- and conduction band remains undisturbed flat. The Fermi energy is given by the acceptor concentration, case a in Fig. 2, valence band and conduction band are shown as solid lines. For 1/10 of the acceptor concentration the band bending reaches the middle of the crystal, shown as case b with dashed lines for conduction and valence band. Reducing the acceptor concentration further to 1/50 of the initial concentration is leading to a band diagram shown as solid line (case c) in the figure. It only slightly differs from a flat condition. The Fermi level now is determined exclusively by the donor level located in the middle of the band gap outside the grain, E_D. Also shown in Fig. 2 are the effective

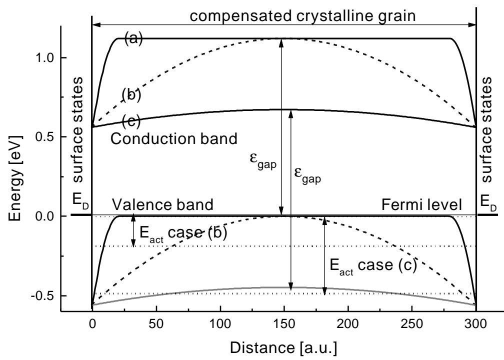

Figure 2: Calculated one dimensional band diagram as a function of the distance assuming a constant high donor density (units are arbitrarily chosen) located at the grain boundaries (x=0 and x=300) and three compensating acceptor concentrations equally distributed within the crystal (0<x<300). Case (a) shows the effect of a high acceptor concentration, For (b) the concentration was 1/10 and for (c) 1/50 of the initial concentration.

energy edges of the valence band as dotted lines. The displayed energy differences, E_{act}, between the Fermi energy and the constant effective valence band edge can be observed as thermal activation energy in temperature dependent conductance measurements.

In Fig. 3 the result of the one dimensional calculation for a variety of acceptor concentration with constant grain diameter and surface concentration on E_{act} is shown. E_{act} is plotted on the x-axis. On the left y-axis the acceptor concentrations used for the calculations are plotted logarithmically. The solid line displays the calculated dependence. For comparison the experimentally observed activation energy [5] as a function of the boron concentration in μc-Si is plotted on the right y-axis, shown by the circles. The coincidence of the two results was obtained by varying the origin of the right y-axis. The scales of the two ordinates oth-

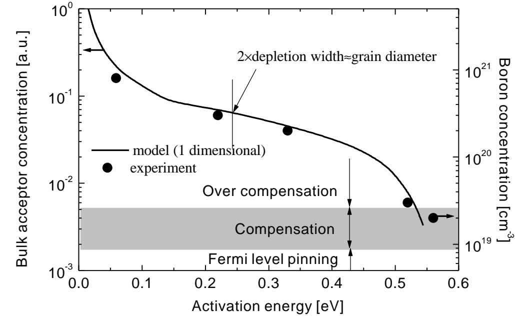

Figure 3: Semilogarithmic plot of the correlation between the activation energy and the compensating acceptor concentration in the bulk. Solid curve and left axis are the calculated results, Circles and right axis are experimentally observed results [5].

erwise are identical, displaying 3 decades. A change of the diameter of the crystallites towards smaller dimensions or a higher surface defect density will shift the curve up to higher acceptor concentrations. An increase of the crystal diameter or a lowering of the surface state density will shift the curve down to lower concentrations.

Three regions can be defined in Fig. 3. For very high doping concentrations (with respect to a constant crystal diameter and a constant surface state density) the crystals are only slightly influenced by the grain boundaries, their properties essentially correspond to those of single crystal material. In this case the activation energy is well below 0.1 eV close to the activation energy of the acceptor level. In Fig. 3 the condition will be true for boron concentrations above 5×10^{20} cm^{-3}. For a wide range of low doping densities the Fermi level is exclusively fixed at the surface state level. In Fig. 3 this is valid for concentrations below 1×10^{19} cm^{-3}. For silicon layers in this regime (E_{act} > 0.5 eV) the information obtainable from electrical measurements about defects is very low. In the intermediate region (1×10^{19} cm^{-3} <N_{Boron}< 5×10^{20} cm^{-3} in Fig. 3) the thermal activation energy is very sensitive to changes of one of the three parameters: crystal diameter, bulk acceptor concentration, surface state density.

From the results of the temperature dependent measurements, the contributions from the noncrystalline and the crystalline phase were extracted. For the hopping conduction a power law was assumed and for the crystals a single thermal activation process in parallel was assumed. The measured capacitance and conductance data were fitted according to these assumptions. Each sample was measured with either the n-ZnO/p-Si junction or the p-Si/undoped Si transition reverse biased. Since in the first case the concentration in the n-ZnO was temperature independent and about one order of magnitude higher than in the p-Si, the depletion region mainly extends into the highly doped p-Si layer. The latter transition was rather graded so that the depletion region only extends partly into the undoped Si but also into the p-Si. While the measured capacitance will solely be determined by the space charge regions, the conductance will be influenced by the whole structure. In Table I the results for the 4 samples are

summarised. Except for the value of E_{act} derived from capacitance measurements for sample D with reverse biased *n*-ZnO/*p*-Si junction in parentheses all values represent mean values.

Table I: Temperature dependence of µc-Si devices determined from capacitance and conductance measurements

sample	crystal: thermally activated (E_{act}) [eV], space charge in Si:B	crystal: thermally activated (E_{act}) [eV], space charge in i-Si	crystal: overall	porous Si hopping: $C \propto T^x$, x	porous Si hopping: $G \propto T^y$, y
A	0.07	0.49	0.42	~0	0.4
B	0.17	0.27	0.17	~0	0.3
C	0.15	0.29	0.25	0.12	~0
D	(0.35)	0.50	0.40	0.02	0.3

As expected for a hopping conduction, capacitance as well as conductance of the noncrystalline, porous phase only vary very little with temperature. No dependence on the preparation conditions was observed. At room temperature, the contribution to the conductance coming from the porous phase, however, was reduced from 5.5% for a substrate temperature of 200 °C (samples A, B) to less than 3% for a substrate temperature of 230 °C (samples C, D). The samples A and D were prepared with a filament temperature of 1600 °C, for samples B and C the temperature was 1800 °C. The activation energy derived from the conductance measurements (overall) as well as the activation energy from capacitance measurements at the *p*-Si/undoped Si junction are significantly different in both cases. As discussed above this change may have several reasons: grain diameter, surface state density, changes in the charge distribution within the depletion region. The observed difference is too large to be explained by a change of the grain size or by the assumption of a less graded junction at the *p*-Si/undoped Si transition. Therefore the assumption that the surface defect density is efficiently reduced is the most likely explanation. According to Fig. 3 a reduction of more than 1 order of magnitude may be estimated.

From the DLTS measurements defect levels were evaluated without corrections for the electrical field dependence or the effect of Fermi level pinning or for multiple impurity centres. Due to the two junctions in the crystallites the depletion region under examination could be located in the boron doped region or in the undoped region of our samples depending on the bias voltage. This allowed us to selectively examine hole traps in *p*-Si and electron traps in the undoped Si. The observed levels and their occurrence in the samples are summarised in Table II. Y denotes levels that have been observed in the sample, the question mark shall indicate the uncertainty whether H_1 and H_2 correspond to the same defect level. Although the energy levels are identical the capture cross sections differ by one order of magnitude. The complex constitutions of the two depletion regions makes it difficult to evaluate the concentrations of the defect levels. A rough estimation suggests that all the observed levels are present in concentrations of less than 10% of the background doping concentration. Since no space charge region is present in the porous fraction no traps could be detected with DLTS.

After applying a temporary surface passivation to sample C the amplitudes of all DLTS signals were reduced below the resolution of our experimental set-up, thus suggesting that the observed defects were rather located at the crystal´s surface than in the bulk.

Table II: Electrically active defects determined by DLTS and their occurrence in different samples.

	Impurity centre: Level	ΔE [eV]	σ_p,σ_n[cm^2]	observed in: A	B	C	D
Hole-Traps	H_1	0.336	2.0×10^{-14}	Y	Y	?	-
	H_2	0.336	2.5×10^{-15}	?	?	Y	-
	H_3*)	0.233	1.5×10^{-17}	-	Y	Y	-
	H_4	0.135	3.0×10^{-18}	Y	-	Y	-
	H_5	0.082	3.5×10^{-20}	Y	-	Y	-
Electron-Traps	E_1	0.449	5.5×10^{-14}	-	-	-	Y
	E_2	0.381	3.0×10^{-16}	-	Y	Y	-
	E_2	0.054	2.5×10^{-19}	Y	-	-	-

*) Inhomogeneously distributed in the depletion region with higher concentrations towards the junction *n*-ZnO/*p*-Si.

4. CONCLUSIONS

From our investigations we conclude that the electrical properties of the deposited µc-Si films can be controlled very accurately by the variation of the deposition parameters. Currently, the observed high density of surface defects present in the layers appear to be the major limitation for the preparation of a high efficient solar cell. Although the condition for the intrinsic material $n \approx p$ where n and p are the electron and hole concentration, respectively, is fulfilled in the undoped layer, the high defect concentration will significantly reduce carrier mobility as well as lifetime below values necessary for a high collection efficiency of light-generated carriers within the absorber. The low possible concentration difference in the doping levels between the *p*-Si or *n*-Si and the "intrinsic" Si (only about 2 orders of magnitude) prohibit the formation of a high built-in drift field which will further reduce the drift field enhanced collection efficiency and the open circuit voltage of a *pin*-device. If a reduction of the surface states of more than one order of magnitude cannot be achieved during the deposition a suitable surface passivation process may be applied.

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